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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,649	ROTH ET AL	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Hohl et al, U.S. Patent Number 6,035,422 (herein referred to as Hohl).

2. Referring to claim 1 Hohl has taught a method comprising:

selecting one of a plurality of debugging modes as a function of a current operating mode of a processor (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging);

invoking one of a plurality of debug handlers, wherein the plurality of debug handlers includes a first debug handler and a second debug handler (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9; Hohl provides both emulation and single-stepping, which would require different handling methods from the debugging system, since the same logic, or code, would not be used for both emulation and single-stepping).

3. Referring to claim 2 Hohl has taught further comprising raising an exception after executing an instruction (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

4. Referring to claim 3 Hohl has taught further comprising invoking an emulation mode of the processor after executing an instruction (Hohl column 27 lines 57-column 28 line 20).

5. Referring to claim 4 Hohl has taught wherein selecting the debugging mode comprises selecting a first debugging mode when the operating mode comprises user mode, and selecting a second debugging mode when the operating mode comprises supervisor mode (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9, column 3 lines 45-63, column 8 lines 36-52; Hohl provides both emulation in a supervisory mode and debugging in a user mode).

6. Referring to claim 5 Hohl has taught a method comprising:

receiving an instruction;

receiving a signal;

selecting a mode of debugging as a function of the signal, wherein selecting the debugging mode comprises selecting a first de bugging mode when the signal is a first signal, and selecting a second debugging mode when the signal is a second signal (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging);

invoking one of a plurality of debug handlers, wherein the plurality of debug handlers includes a first debug handler and a second debug handler (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9; Hohl provides both emulation and single-stepping, which would require different handling methods from the debugging system, since the same logic, or code, would not be used for both emulation and single-stepping); and

executing the instruction.

7. Referring to claim 6 Hohl has taught further comprising raising an exception (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

8. Referring to claim 7 Hohl has taught further comprising invoking an emulation event (Hohl column 27 lines 57-column 28 line 20).

9. Referring to claim 8 Hohl has taught further comprising:

sensing register contents (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method); and

outputting register contents (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54).

10. Referring to claim 9 Hohl has taught wherein the instruction is received by a processor adapted to operate in a plurality of states, the method further comprising:

sensing states of the processor (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method); and

outputting states of the processor (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54).

11. Referring to claim 10 Hohl has taught wherein the instruction is received by a processor, the method further comprising selecting a mode of single-step debugging as a function of the operating mode of the processor (column 12 lines 1-9, column 3 lines 45-63, column 8 lines 36-52).

12. Referring to claim 11 Hohl has taught a device comprising:

a processor, the processor adapted to operate in a plurality of operating modes including an emulation mode (Hohl column 27 lines 57-column 28 line 20);

a control register adapted to store the state of a control bit (Hohl); and

a plurality of debug handlers, wherein the plurality of debug handlers includes a first debug handler and a second debug handler (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9; Hohl provides both emulation and single-stepping, which would require different handling methods from the debugging system, since the same logic, or code, would not be used for both emulation and single-stepping);

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the control bit (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user controls the debugging).

13. Referring to claim 12 Hohl has taught wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user

controls the debugging; the system checks certain bits in registers to determine the mode, and debug method).

14. Referring to claim 13 Hohl has taught further comprising exception logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

15. Referring to claim 15 Hohl has taught wherein the control bit is a first control bit, the system further comprising a second control bit, and wherein the mode of single-step debugging is a function of the state of the second control bit (column 12 lines 1-9, column 3 lines 45-63, column 8 lines 36-52).

16. Referring to claim 16 Hohl has taught wherein the processor is a digital signal processor (Hohl abstract, background; Hohl uses an environment using digital signals).

17. Referring to claim 17 Hohl has taught a device comprising:

a processor, the processor adapted to operate in a plurality of operating modes ;

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging) and wherein the processor is further adapted to invoke one of a plurality of debug handlers, wherein the plurality of debug handlers includes a first debug handler and a second debug handler (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9; Hohl provides both emulation and single-stepping, which would require different

handling methods from the debugging system, since the same logic, or code, would not be used for both emulation and single-stepping).

18. Referring to claim 18 Hohl has taught further comprising a control register adapted to store the state of a control bit (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method),

wherein the processor is adapted to select one of the plurality of debugging modes as a function of the state of the control bit (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method).

19. Referring to claim 19 Hohl has taught further comprising:

an exception handler (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52); and

logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

20. Referring to claim 21 Hohl has taught wherein the processor is a digital signal processor (Hohl abstract, background; Hohl uses an environment using digital signals).

21. Referring to claim 22 Hohl has taught a system comprising:

a processor, the processor adapted to operate in a plurality of operating modes (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9);

a control register adapted to store the state of a control bit (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9);

an input/output device (Hohl figure 1, column 3 lines 45-63, column 8 lines 36-52); and

a plurality of debug handlers, wherein the plurality of debug handlers includes a first debug handler and a second debug handler (Hohl column 27 lines 57-column 28 line 20; column 12 lines 1-9; Hohl provides both emulation and single-stepping, which would require different handling methods from the debugging system, since the same logic, or code, would not be used for both emulation and single-stepping);

wherein the processor is to adapted to select one of a plurality of debugging modes as a function of the control bit (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54; shows the difference between emulation in a supervisory mode, and when the user controls the debugging).

22. Referring to claim 23 Hohl has taught wherein the processor is adapted to select one of a plurality of debugging modes based upon the current operating mode (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method).

23. Referring to claim 24 Hohl has taught further comprising a memory device coupled to the processor (Hohl figure 1).

24. Referring to claim 25 Hohl has taught further comprising logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

25. Referring to claim 27 Hohl has taught wherein the control bit is a first control bit, the system further comprising a second control bit, wherein the processor is adapted to select one of a plurality of debugging modes based upon the state of the second control bit (Hohl column 9 line 23-column 10 lines 34, column 12 lines 47-54, column 13 lines 15-20, column 8 lines 36-52; shows the difference between emulation in a supervisory mode, and when the user controls the debugging; the system checks certain bits in registers to determine the mode, and debug method).

26. Referring to claims 14, 20, and 26 Hohl has taught further comprising logic adapted to sense the state of the control bit and to trigger an emulation event as a function of the state of the control bit (Hohl column 27 lines 57-column 28 line 20).

27. Referring to claims 28 and 31 Hohl has taught wherein the first debug handler is capable to debugging the second debug handler (Hohl column 27 lines 57-column 28 line 20; the emulation mode has all of the supervisor privileges, and restricted access).

28. Referring to claim 29 Hohl has taught wherein the first debug handler is an emulation service routine (Hohl column 27 lines 57-column 28 line 20).

29. Referring to claim 30 Hohl has taught wherein the second debug handler is an exception handler (Hohl column 12 lines 1-9, column 2 lines 22-34, column 8 lines 36-52; an interrupt and

exception serve the same function, as they both stop the normal operation of the processor, and in this case for "debugging" purposes).

Response to Arguments

30. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

September 27, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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